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(54) **Method and apparatus for automatic tuning calibration of electronically tuned filters.**

(57) A method and apparatus (11) for automatic tuning calibration of electronically tuned filters (12, 16) which comprises a programmable frequency generator (20, 18, 30) for producing a calibration frequency signal, a filter (16) for filtering the calibration frequency signal, a detector (26, 24) for producing a detector voltage (V_{DET}), a processor (22, 23) for programming the frequency generator (20, 18, 30) to specific test frequencies and for producing a stepped filter tuning voltage (V_{T1}, V_{T2}) and storing the detector voltage (V_{DET}) in response to the stepped filter tuning voltage (V_{T1}, V_{T2}), and a converter (28) for digital-to-analog conversion of the stepped filter tuning voltage (V_{T1}, V_{T2}). Calibration frequency signal (F_S) versus tuning voltage responses are stored for a number of calibration iterations within the usable range of the filter (16) and the resulting table can be used to determine the correct tuning voltage (V_{TS1}) for the filter (16) when operating at any frequency within the usable filter range.

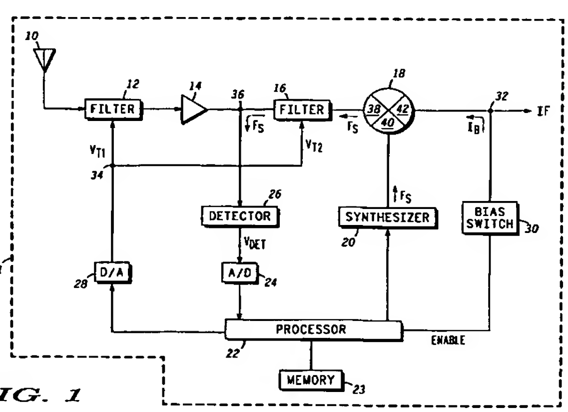

FIG. 1

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BACKGROUND OF THE INVENTION

This invention relates in general to the field of tuning calibration, and in particular to the automatic tuning calibration of electronically tuned filters.

Electronically tuned radio frequency (RF) filters such as those implemented with varactors produce varying tuning characteristics, e.g., frequency versus voltage variations, that are a function of a number of variables. Varying tuning characteristics can arise from variability in component tolerances, printed wiring board dimensions and the dielectric constant of the board material, stray inductance and capacitance variations due to component and shield or ground plane placement.

Many equipment designs in which electronically tuned filters are used contain microprocessor controllers and non-volatile memory capability. Typical filter calibration techniques do not take advantage of these additional components in addressing the filter calibration problem in electronically tuned filters.

Among typical approaches used to calibrate electronically tuned filters are adjustable RF components used to "trim" the filter to track a predetermined tuning curve, adjustable or select-in-test components in an analog tracking circuit to interface a standard voltage versus frequency curve to the individual characteristics of the filter, and components with very accurate value tolerances. These techniques are expensive in terms of test labor required and/or component cost.

Another approach to address electronically tuned filter calibration is an active approach which measures the phase shift between an applied test signal and the filter output and which provides a unique null output indicating correct tuning of the filter. This active servo loop technique is relatively elaborate and more expensive, however, requiring several directional couplers and a phase detector and higher signal levels for proper operation as a result.

A need exists, therefore, for a method and apparatus for automatic tuning calibration of electronically tuned filters which requires relatively few components, is relatively inexpensive, and does not require adjustments at the factory. The approach should be applicable in RF equipment such as transmitters, receivers, or test equipment that require electronically tuned filters and include programmable RF sources and microprocessor-controlled systems. The approach should reduce the cost of the filters and provide precise tuning of very narrow bandwidth filters that might not otherwise be feasible due to the high tracking accuracy required.

SUMMARY OF THE INVENTION

Accordingly, it is an advantage of the present invention to provide a new and improved method and apparatus for automatic tuning calibration of electronically tuned filters which takes advantage of programmable RF sources and microprocessor-controlled systems. It is an additional advantage that the method and apparatus for automatic tuning calibration is generally applicable to transmitters, receivers, and/or test equipment, yet requires relatively few components and is relatively inexpensive. It is still further an advantage of the present invention the method and apparatus for automatic tuning calibration of electronically tuned filters provides precise tuning of very narrow bandwidth filters that might not otherwise be feasible due to the high tracking accuracy required.

To achieve these advantages, a method and apparatus for automatic tuning calibration of electronically tuned filters is contemplated which comprises a programmable frequency generator for producing a calibration frequency signal, a filter for filtering the calibration frequency signal, a detector for producing a detector voltage, a processor for programming the frequency generator to specific test frequencies and for producing a stepped filter tuning voltage and storing the detector voltage in response to the stepped filter tuning voltage, and a converter for digital-to-analog conversion of the stepped filter tuning voltage.

Calibration frequency signal versus tuning voltage responses are stored for a number of calibration iterations within the usable range of the filter. The calibration frequency signal versus tuning voltage table is then used to determine the correct tuning voltage for the filter for any frequency within the usable range of the filter.

The above and other features and advantages of the present invention will be better understood from the following detailed description taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

In FIG. 1, there is shown a schematic circuit diagram of a circuit for automatic tuning calibration of electronically tuned filters in a radio receiver in accordance with a preferred embodiment of the invention.

In FIG. 2, there is a representative graph of a detector voltage versus tuning voltage curve for a particular test signal (synthesizer frequency).

In FIG. 3, there is a flowchart representation of a method of automatic tuning calibration of electronically tuned filters in accordance with a preferred embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. 1 illustrates schematically the diagram of a circuit for automatic tuning calibration of electronically tuned filters. The approach can be applied in RF equipment such as transmitters, receivers, or test equipment, i.e., any application using electronically tuned filters and possessing programmable RF sources and microprocessor controlled systems. The FIG. 1 application represents the method and apparatus applied to the radio receiver 11.

In FIG. 1, antenna 10 is coupled to filter 12. Filter 12 is coupled through amplifier 14 to junction 36. Junction 36 is coupled both through filter 16 to R port 38 of mixer 18 and through detector 26 to converter 24. Converter 24 is coupled to processor 22. Processor 22 is coupled through converter 28 to junction 34. Memory 23 is coupled to processor 22. Junction 34 is coupled to filter 12 and also to filter 16.

Processor 22 is also coupled through synthesizer 20 to L port 40 of mixer 18. Processor 22 is also coupled through bias switch 30 to junction 32. Junction 32 is coupled to the I port 42 of mixer 18. Junction 32 serves as the intermediate frequency (IF) output.

Filters 12 and 16 in the preferred embodiment are to be essentially identical filters. Filters 12 and 16 exhibiting identical performance characteristics allows the tuning calibration measurements to test filter 16, but apply the tuning voltages resulting from the tuning calibration measurements to the receiver filter 12. Should the filters not be identical, or it be desirable to characterize the tuning characteristics of filter 12 directly, filter 12 may be calibrated in a manner similar to the calibration of filter 16.

In operation, the FIG. 1 circuit automatically determines the correct tuning voltage for tuning the receiving tuning filter 12 in the following way. Processor 22 enables bias switch 30 to a bias (direct) current, i.e., I_B, through junction 32 to the I port 42 of diode balanced mixer 18. Mixer 18, responding to the bias current at the I port 42, connects R port 38 to L port 40 of mixer 18.

Processor 22 simultaneously executes a program using synthesizer 20 to generate a test signal, i.e., a synthesizer signal at frequency F_S. When R port 38 of mixer 18 is connected to L port 40 of mixer 18, test signal F_S is input into filter 16. The test signal F_S passes through filter 16 to junction 36, and then into detector 26.

Processor 22 transmits a digital tuning voltage to converter 28. Converter 28, a digital-to-analog converter, creates an analog tuning voltage signal from the digital tuning voltage of processor 28 and applies the analog tuning voltage V_{T2} to junction 34 and, thus, to filter 16. At junction 34, the analog tuning voltage is also input into filter 12 as V_{T1}. The tuning voltages V_{T1} and V_{T2} are identical.

Filter 16 produces an output based on the synthesizer signal at frequency F_S and the tuning voltage V_{T2} input to filter 16. The filter 16 output is received by the detector 26, which produces a detected voltage, V_{DET}, in response.

Processor 22 sets the first synthesizer frequency, F_{S1}, to a first calibration frequency, i.e., the lowest filter frequency for both filters 12 and 16. While producing the fixed test signal, F_{S1}, processor 22 also produces the digital tuning voltage signal in steps. The stepped digital tuning voltage produces a range of analog tuning voltages from converter 28, which in turn produces a series of detected analog voltages, V_{DET}, from detector 26.

FIG. 2 illustrates what curve the detected voltage, V_{DET},versus tuning voltage, V_{T1} or V_{T2}, shown on the abscissa as V_{TUNE}, might trace for filter 12 or filter 16. The detected voltage rises as the tuning voltage is increased, reaches a relative local maximum, and decreases. The local maximum occurs when the tuning voltage $V_{TUNE} = V_{PK}$, and V_{LOW} and V_{HIGH} are defined as the tuning voltages giving rise to detector voltage values of $0.7V_{DET}$ maximum.

The FIG. 1 circuit processes the FIG. 2 information as follows. Processor 22, receiving a digital version of the detected voltage from detector 26 through converter 24, stores the detected voltage corresponding to each tuning step in the memory 23. The processor stores the tuning voltage corresponding to the maximum detected voltage as V_{PK}. Processor 22 continues to step the tuning voltage until the detected voltage drops below a value of $0.7V_{PK}$. This value was chosen for the preferred embodiment but can be chosen differently, depending on the desired application and effect, without affecting the operation of the automatic filter calibration method. Processor 22 stores the tuning voltage corresponding to $V_{DET} = 0.7V_{PK}$ as V_{HIGH} in memory 23. Processor 22 then examines previously stored detector voltages from tuning voltages less than V_{PK} and defines the tuning voltage that precedes the first step where V_{DET} was greater or equal to $0.7V_{PK}$ as V_{LOW}. V_{LOW} is also stored in memory 23.

Processor 22 in this preferred embodiment using a relatively narrow bandwidth filter then calculates the correct tuning voltage for frequency F_{S1} using the equation:

$$V_{TSi} = (V_{LOW} - V_{HIGH})/2 + V_{CORR} \quad \text{(Equation 1)}$$

where $i = 1$. V_{CORR} is an empirical correction factor

from a look-up table stored in memory 23, and represents a tuning voltage correction based on the particular filter shape and filter center frequency used. The use of V_{CORR} allows the processor 22 to set a tuning voltage slightly off the passband center frequency to optimize for other considerations, such as stopband symmetry or maximum high side or low side rejection, etc., if so desired. The processor 22 stores V_{TS1} as the correct tuning voltage at frequency F_{S1}. (Depending on how narrow the band of filter 12 or 16, processor 22 could also calculate the tuning voltage using another algorithm, e.g., as the geometric mean of V_{LO} and V_{HIGH}.)

Processor 22 sets a next calibration frequency, F_{S2}, i.e., a step up from the lowest filter frequency for both filters 12 and 16. While the synthesizer produces the fixed test signal, F_{S2}, processor 22 also produces the digital tuning voltage in steps. The stepped digital tuning voltage produces a range of analog tuning voltages from converter 28, which in turn produces another series of detected analog voltages, V_{DET}, from detector 26 for the second test signal, F_{S2}. In the same manner described for determining V_{PK}, V_{LOW}, and V_{HIGH} for the first test signal, F_{S1}, new V_{PK}, V_{LOW}, and V_{HIGH} values are generated for F_{S2} by processor 22 and stored in memory 23.

The same calibration process is repeated for test signals F_{S3} through F_{SN}, with F_{SN} being the highest usable frequency of the filters 12 and 16. The number of calibration iterations, N, can be varied, depending on the tuning range and the linearity of the responses of filters 12 and 16 over that range. A correct tuning voltage, V_{TSi}, is therefore generated and stored for each test signal F_{Si} throughout the usable frequencies of filters 12 and 16.

The list, or table, of correct tuning voltages versus frequency stored in memory 23 can be used to calibrate filter 16 when operated as a receiver filter in FIG. 1. The antenna in FIG. 1 receives an external signal which is transmitted to filter 12. The correct tuning voltage for any operating frequency F_X within the operational frequency limits of filter 12, i.e., from F_{S1} to F_{SN}, is calculated by linear interpolation by processor 22 using the two tuning voltage calibration points closest in frequency to F_X.

FIG. 3 illustrates the automatic filter tuning approach method applying to the circuit in FIG. 1. The bias switch 30 is enabled by the processor 22, as shown in box 50 of FIG. 3. The bias current I_B is applied to mixer 18, as shown in box 52. Synthesizer 20 is programmed by processor 22 to produce a signal at the lowest usable frequency of filters 12 and 16. Synthesizer 20 produces a signal at frequency F_S, illustrated in box 53. The synthesizer signal at frequency F_S is transmitted to filter 16, as shown in box 54. Box 56 of FIG. 3 shows the filtering of the synthesizer signal, and boxes 58 and 60 describe detection and digitization, respectively, of the resulting detector voltage.

Processor 22 reads and stores the digitized detector voltage V_{DET}, as shown in box 62. Processor 22 also steps the tuning voltage to filter 16, as shown in box 64. If the detector voltage read for the current tuning voltage step is not the maximum detector voltage, box 66 transfers control to box 64 via the NO path and the system continues to step the filter tuning voltage to find the maximum voltage. If the detector voltage read for the current tuning voltage step is the maximum detector voltage, that maximum value is stored in the memory 23 as V_{PK}, as shown by box 66 transferring control to box 67, proceeding on the YES path.

In box 68, the filter tuning voltage continues to be stepped to locate V_{HIGH}, which is the tuning voltage for which the detected voltage has decreased from V_{PK} to $0.7V_{PK}$. If the detected voltage V_{DET} is not V_{HIGH}, control is transferred from box 69 to box 68 via the NO path and the system continues stepping the tuning voltage. If, however, the current V_{DET} is equal to V_{HIGH}, then via the YES path, box 69 is taken to box 70 and V_{DET} is stored in memory 23 as V_{HIGH}, as shown in box 70.

V_{LOW} is determined by the processor 22 comparing previously stored V_{DET} values in memory 23 with V_{PK}. V_{LOW} is set equal to the tuning voltage that precedes the first tuning voltage step where V_{DET} was greater or equal to $0.7V_{PK}$, as shown in box 71.

The empirical correction factor V_{CORR} is read from the memory 23 as shown in box 72, and, as shown in box 74, processor 22 calculates and stores the tuning voltage value for the particular synthesizer frequency F_{Si} using equation 1.

If the current F_S is not the highest usable filter 16 frequency, control is transferred from box 76 via the NO path to box 78 where a new synthesizer frequency F_S is generated. Control is transferred to box 54, and the F_S signal at the new synthesizer frequency is sent to filter 16. The system repeats e steps shown in the flowchart boxes to calculate the tuning voltage V_{TS} for the new F_S.

If F_S is the highest usable filter 16 frequency, control is transferred from box 76 to box 80 via the YES path, and the tuning voltage versus frequency table is complete and stored in memory 23. For any operational frequency F_X as shown in box 82, F_X can be looked up in the tuning voltage table, as shown in box 84. As shown in box 86, linear interpolation can be used to locate the proper tuning voltage for F_X between any two frequency values in the table. The tuning voltage corresponding to the operating frequency F_X can then

be used to calibrate filter 16 (or filter 12), as shown in box 88. The process is complete.

Thus, there has been described a method and apparatus for automatic tuning calibration of electronically tuned filters which overcomes specific problems and accomplishes certain advantages relative to prior art methods and mechanisms. The improvements are significant. The method and apparatus for automatic tuning calibration of electronically tuned filters requires relatively few components, is relatively inexpensive, and does not require adjustments at the factory. The approach is applicable to RF equipment such as transmitters, receivers, or test equipment that require electronically tuned filters and possess programmable RF sources and microprocessor-controlled systems. The approach reduces the cost of the filters and provides precise tuning of very narrow bandwidth filters that might not otherwise be feasible due to the high tracking accuracy required.

Thus, there has also been provided, in accordance with an embodiment of the invention, a method and apparatus for automatic tuning calibration of electronically tuned filters which overcomes specific problems and accomplishes certain advantages and which fully satisfies the aims and advantages set forth above. While the invention has been described in conjunction with a specific embodiment, many alternatives, modifications, and variations will be apparent to those of ordinary skill in the art in light of the foregoing description. Accordingly, the invention is intended to embrace all such alternatives, modifications, and variations as fall within the spirit and broad scope of the appended claims.

Claims

1. An automatic tuning calibrator (11) for electronically tuned filters (12, 16) comprising:

   programmable frequency generator means (20, 18, 30) for producing (53) a calibration frequency signal;

   filter means (16) for filtering (54) the calibration frequency signal, the filter means (16) coupled to the frequency generator means (20, 18, 30);

   detector means (26, 24) for producing (58) a detector voltage (V_{DET}), the detector means (26, 24) coupled to the filter means (16);

   processor means (22, 23) for producing (64, 66) a stepped filter tuning voltage (V_{T1}, V_{T2}) and for storing (67) the detector voltage (V_{DET}) in response to the stepped filter tuning voltage (V_{T1}, V_{T2}), the processor means (22, 23) coupled to the detector means (26, 24) and to the frequency generator means (20, 18, 30); and

   converter means (28) for digital-to-analog conversion of the stepped filter tuning voltage (V_{T1}, V_{T2}), the converter means (28) coupled to the processor means (22, 23) and to the filter means (16).

2. An automatic tuning calibrator (11) as claimed in claim 1, wherein the frequency generator means (20, 18, 30) comprises:

   synthesizer means (20) for producing (53) the calibration frequency signal;

   mixer means (18) for connecting the synthesizer means (20) to the filter means (16), the mixer means (18) coupled to the synthesizer means (20) and to the filter means (16); and

   bias switch means (30) for enabling (50, 52) the mixer means (18), the bias switch means (30) coupled to the mixer means (18) and to the processor means (22, 23).

3. An automatic tuning calibrator (11) as claimed in claim 2, wherein the detector means (26, 24) comprises:

   analog voltage detector means (26) for detecting (58) the filtered calibration frequency signal and for producing (58) an analog detector voltage output, the analog voltage detector means (26) coupled to the filter means (16); and

   analog-to-digital converter means (24) for producing (60) the detector voltage output from the analog voltage output, the analog-to-digital converter means (24) coupled to the analog voltage detector means (26) and to the processor means (22, 23).

4. An automatic tuning calibrator (11) as claimed in claim 2, wherein the processor means (22, 23) comprises:

   storage means (23) for recording (62) the digitized detector voltage output; and

   microprocessor means (22) for enabling (50, 52) the bias switch means (18), for programming (53, 64, 68) the synthesizer means (20), for producing (64, 68) a stepped filter tuning voltage (V_{T1}, V_{T2}), and for determining (64-88) a calculated tuning voltage (V_{TS1}) from the detector voltage (V_{DET}), the microprocessor means (22) coupled to the storage means (23).

5. An automatic tuning calibrator (11) as claimed in claim 4, wherein the storage means (23) comprises non-volatile memory (23).

6. An automatic tuning calibrator (11) for tuning electronically tuned filters (12, 16) in a radio

receiver (11), the automatic tuning calibrator (11) comprising:

programmable frequency generator means (20, 18, 30) for producing (53) a calibration frequency signal;

first filter means (16) for producing (54) a filtered calibration frequency signal from the calibration frequency signal, the first filter means (16) coupled to the frequency generator means (20, 18, 30);

detector means (26, 24) for producing (58, 60) a detector voltage (V_{DET}), the detector means (26, 24) coupled to the first filter means (16);

processor means (22, 23) for producing (64, 68) a stepped filter tuning voltage (V_{T1}, V_{T2}) and for storing (67, 70) the detector voltage (V_{DET}) in response to the stepped filter tuning voltage (V_{T1}, V_{T2}), the processor means (22, 23) coupled to the detector means (26, 24) and to the frequency generator means (20, 18, 30);

converter means (28) for digital-to-analog conversion of the stepped filter tuning voltage (V_{T1}, V_{T2}), the converter means (28) coupled to the processor means (22, 23) and to the first filter means (16); and

radio receiver means (10, 12, 14) for receiving an operating frequency signal, the radio receiver means (10, 12, 14) coupled to the first filter means (16), to the detector means (26, 24), and to the converter means (28).

7. An automatic tuning calibrator (11) as claimed in claim 6, wherein the frequency generator means (20, 18, 30) comprises:

synthesizer means (20) for producing (53) the calibration frequency signal;

mixer means (18) for connecting the synthesizer to the first filter means (16), the mixer means (18) coupled to the synthesizer means (20) and to the first filter means (16); and

bias switch means (30) for enabling (50, 52) the mixer means (18), the bias switch means (30) coupled to the mixer means (18) and the processor means (22, 23).

8. An automatic tuning calibrator (11) as claimed in claim 6, wherein the detector means (26, 24) comprises:

analog voltage detector means (26) for detecting (58) the filtered calibration frequency signal and for producing an analog voltage output, the analog voltage detector means (26) coupled to the first filter means (16); and

analog-to-digital converter means (24) for producing (60) the detector voltage output from the analog voltage output, the analog-to-digital converter means (24) coupled to the analog voltage detector means (26) and to the processor means (22, 23).

9. An automatic tuning calibrator (11) as claimed in claim 7, wherein the processor means (22, 23) comprises:

non-volatile memory (23) for recording the detector voltage (V_{DET}); and

microprocessor means (22) for enabling (50, 52) the bias switch means (18), for programming (53) the synthesizer means (20), for producing (64, 68) a stepped filter tuning voltage (V_{T1}, V_{T2}), and for determining (64-88) a calculated tuning voltage (V_{TS1}) from the detector voltage (V_{DET}), the microprocessor means (22) coupled to the storage means (23).

10. A method for automatic tuning calibration of electronically tuned filters (12, 16) comprising the steps of:

producing (53) a calibration frequency signal in a programmable frequency generator (20, 18, 30);

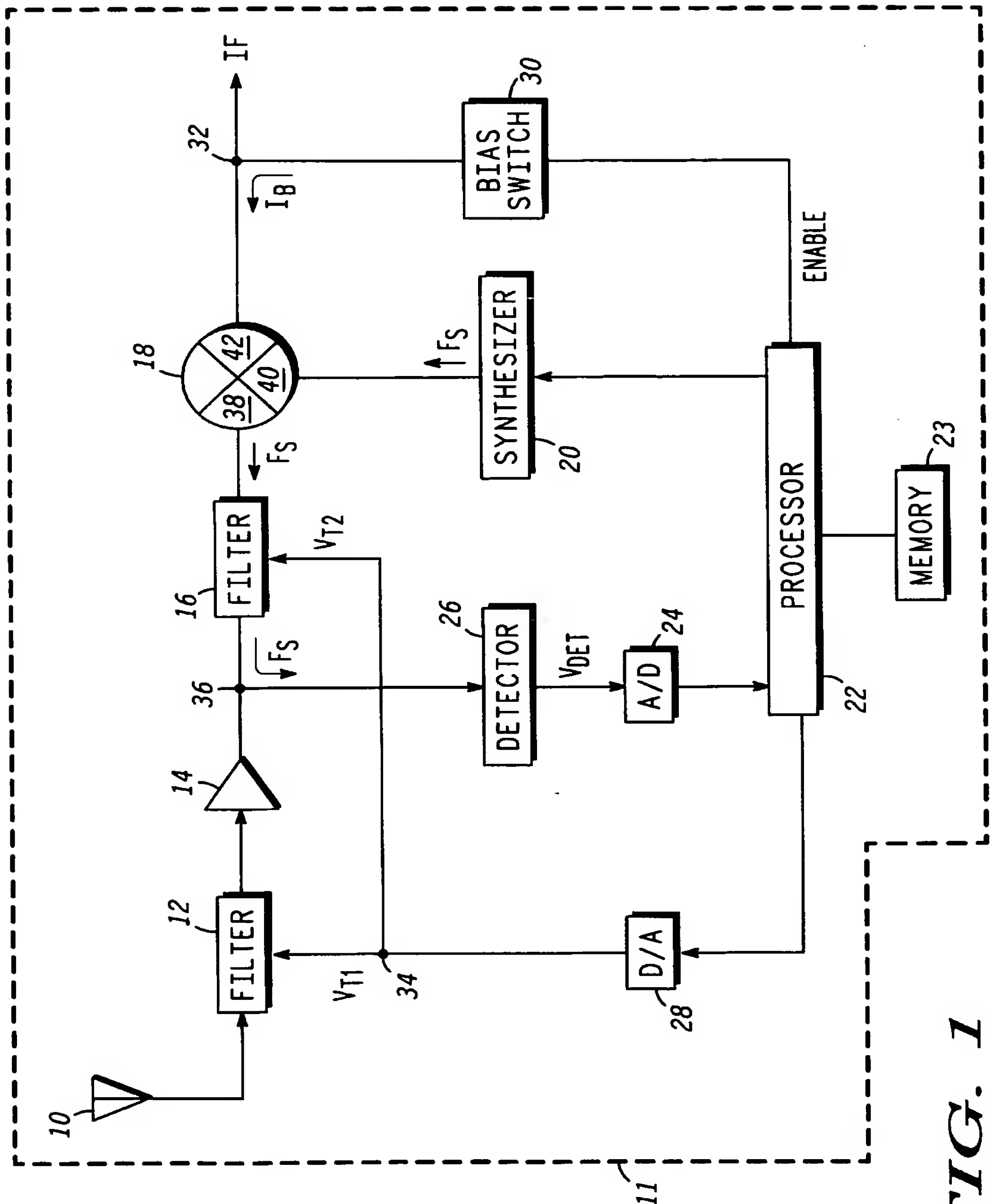
producing (56) a filtered calibration frequency signal from the calibration frequency signal in a first filter (16);

producing (58) a detector voltage (V_{DET}) in a detector (26, 24);

producing (64, 68) a stepped filter tuning voltage (V_{T1},V_{T2}) in a processor (22, 23);

storing (67, 70) the detector voltage (V_{DET}) in response to the stepped filter tuning voltage (V_{T1}, V_{T2}) in the processor (22, 23); and

calculating (74-88) a filter tuning voltage (V_{TS1}) from the detector voltage (V_{DET}) in the processor (22, 23).



IF
32
I_B
BIAS SWITCH
30
ENABLE
SYNTHESIZER
20
F_S
18
42
40
38
FILTER
16
V_{T2}
DETECTOR
26
V_{DET}
A/D
24
PROCESSOR
22
MEMORY
23
36
14
FILTER
12
V_{T1}
34
D/A
28
10
11

FIG. 1

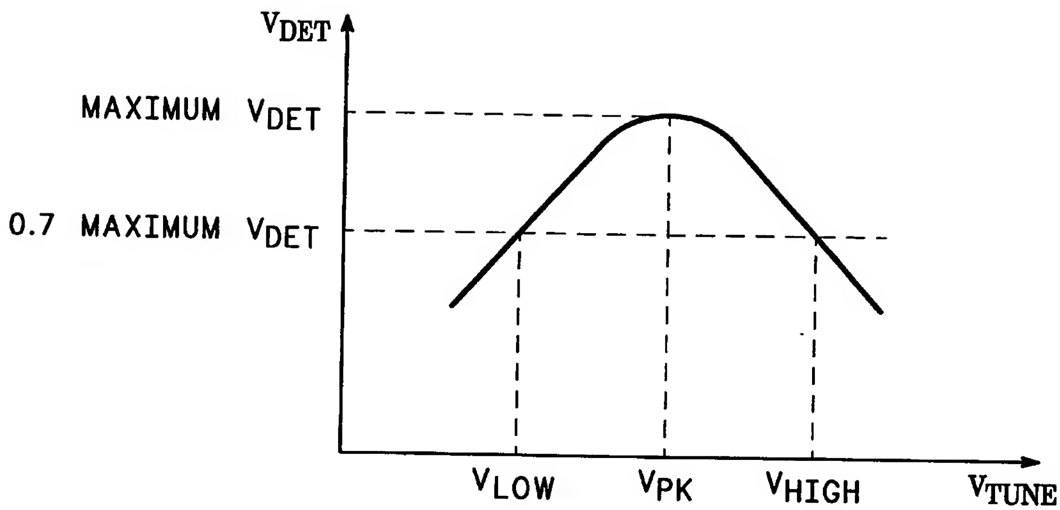


FIG. 2

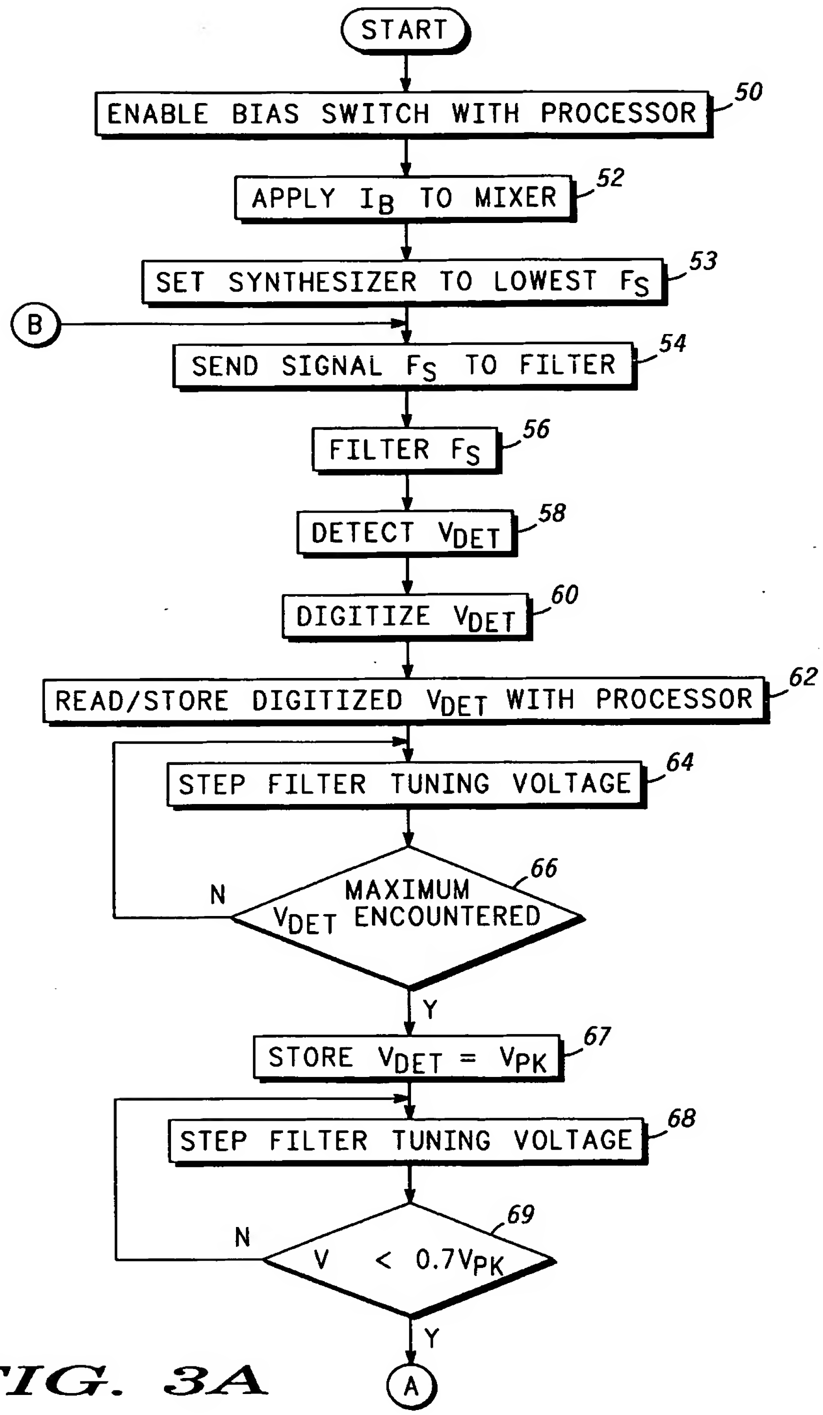

START
ENABLE BIAS SWITCH WITH PROCESSOR
50
APPLY I_B TO MIXER
52
SET SYNTHESIZER TO LOWEST F_S
53
B
SEND SIGNAL F_S TO FILTER
54
FILTER F_S
56
DETECT V_{DET}
58
DIGITIZE V_{DET}
60
READ/STORE DIGITIZED V_{DET} WITH PROCESSOR
62
STEP FILTER TUNING VOLTAGE
64
MAXIMUM V_{DET} ENCOUNTERED
66
N
Y
STORE $V_{DET} = V_{PK}$
67
STEP FILTER TUNING VOLTAGE
68
V < $0.7V_{PK}$
69
N
Y
A

FIG. 3A

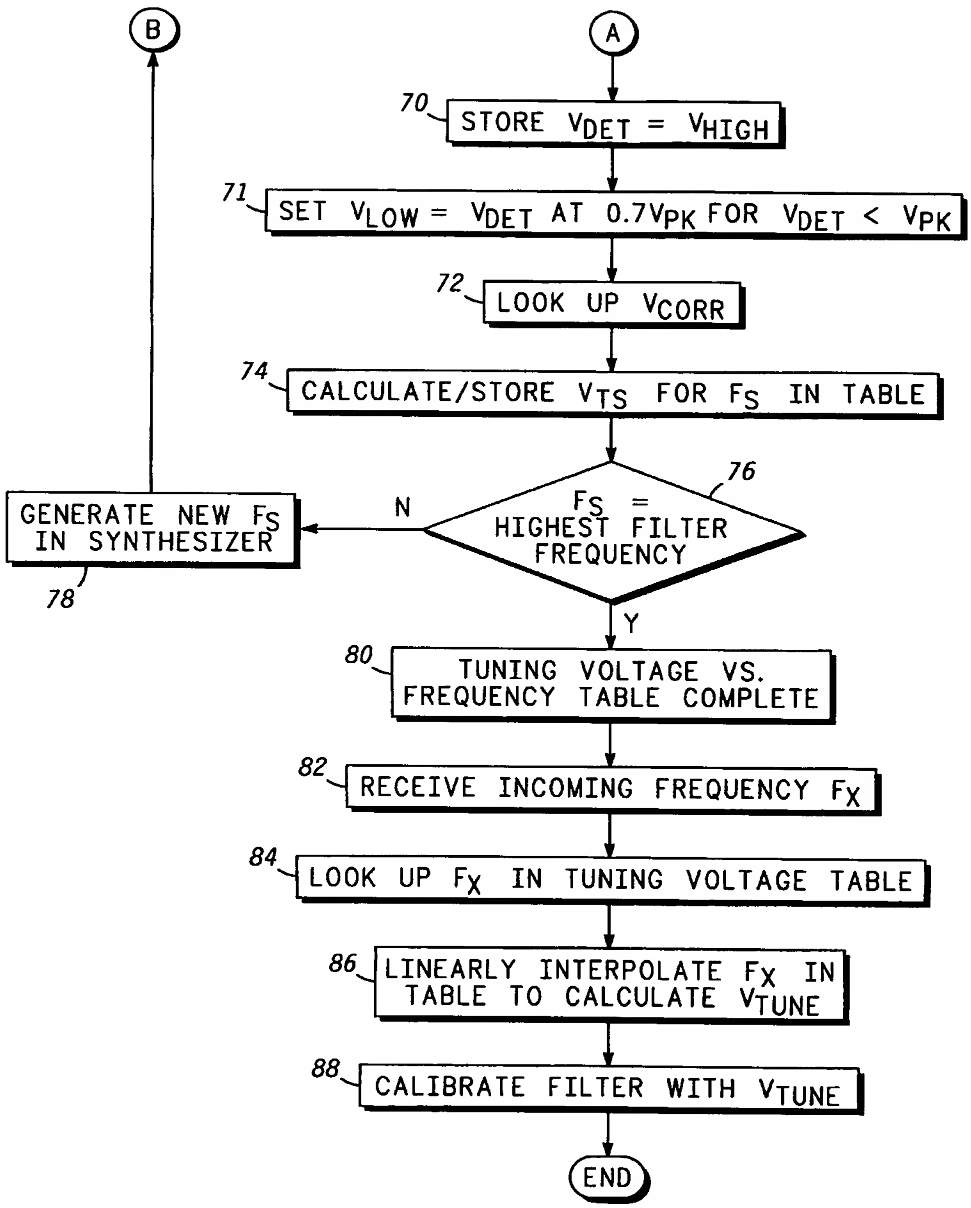

B
A
70
STORE VDET = VHIGH
71
SET VLOW = VDET AT 0.7VPK FOR VDET < VPK
72
LOOK UP VCORR
74
CALCULATE/STORE VTS FOR FS IN TABLE
76
FS = HIGHEST FILTER FREQUENCY
N
GENERATE NEW FS IN SYNTHESIZER
78
Y
80
TUNING VOLTAGE VS. FREQUENCY TABLE COMPLETE
82
RECEIVE INCOMING FREQUENCY FX
84
LOOK UP FX IN TUNING VOLTAGE TABLE
86
LINEARLY INTERPOLATE FX IN TABLE TO CALCULATE VTUNE
88
CALIBRATE FILTER WITH VTUNE
END

FIG. 3B

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 92 11 7504

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	US-A-4 334 323 (F. MOORE) * column 1, line 53 - column 3, line 21; figure 1 * * column 3, line 41 - line 52; figure 2 *	1,6,8,10	H03J5/02 H03J3/32
X	EP-A-0 116 350 (DEUTSCHE THOMSON-BRANDT GMBH) * page 3, line 1 - line 8 * * page 5, line 3 - page 6, line 10; claims 1,2; figure 1 *	1,6,8,10	
A	EP-A-0 119 561 (DEUTSCHE THOMSON-BRANDT GMBH) * page 4, line 11 - page 5, line 3; figures 1,2 * * page 6, line 13 - line 15 *	1,6,10	
A	EP-A-0 109 661 (DEUTSCHE THOMSON-BRANDT GMBH) * page 4, line 1 - page 5, line 15; claims 1,3; figure 1 *	1,6,10	TECHNICAL FIELDS SEARCHED (Int. Cl.5)
A	EP-A-0 208 470 (MATSUSHITA ELECTRIC INDUSTRIAL CO. LTD) * page 3, line 12 - page 4, line 8 * * page 12, line 13 - page 16, line 19; figure 1 *	1,6,10	H03J

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	04 FEBRUARY 1993	BUTLER N.A.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
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& : member of the same patent family, corresponding document